## COURSE STRUCTURE

### M.E. (Embedded Systems)

<table>
<thead>
<tr>
<th>Subject code</th>
<th>Name of subject</th>
<th>Teaching Scheme Hr/week</th>
<th>Examination Scheme Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>SEMESTER –I</strong></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>MS01</td>
<td>Design with Microcontrollers</td>
<td>3 1 - 4</td>
<td>100 25 - 125</td>
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<tr>
<td>MS02</td>
<td>Advanced Digital System Design</td>
<td>3 1 - 4</td>
<td>100 25 - 125</td>
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<tr>
<td>MS03</td>
<td>Digital Signal Processors &amp; Applications</td>
<td>3 1 - 4</td>
<td>100 25 - 125</td>
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<tr>
<td>MS04</td>
<td>CMOS VLSI Design</td>
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<tr>
<td>MS05</td>
<td>Elective-I</td>
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<td>MS06</td>
<td>System Lab-I</td>
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<td>500 125 25 650</td>
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<tr>
<td><strong>Elective-I</strong></td>
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<tr>
<td>(a)</td>
<td>Image and Video Processing</td>
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<td>(b)</td>
<td>RF and Mixed Signal Integrated Circuits</td>
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<tr>
<td>(c)</td>
<td>Statistical Signal Processing</td>
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<tr>
<td><strong>SEMESTER –II</strong></td>
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<td>MS07</td>
<td>Embedded Systems Design</td>
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<td>MS08</td>
<td>Advanced Computer Architecture</td>
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<td>MS09</td>
<td>VLSI Digital Signal Processing Systems</td>
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<td>MS10</td>
<td>Real Time Operating Systems</td>
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<td>MS11</td>
<td>Elective-II</td>
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<tr>
<td><strong>Elective-II</strong></td>
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<tr>
<td>(a)</td>
<td>Reconfigurable Computing</td>
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<td>(b)</td>
<td>Adaptive Signal Processing</td>
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<td>(c)</td>
<td>Analog Integrated Circuit Design</td>
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<td>Th  TW  P  Total</td>
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<td>--  --  24 24</td>
<td>--  100  --  100</td>
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<td>SEMESTER –IV</td>
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<td>L  T  P  Total</td>
<td>Th  TW  P  Total</td>
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<td>Dissertation</td>
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<td><strong>Grand Total (For all 4 Semester)</strong></td>
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MS01: DESIGNING WITH MICROCONTROLLERS

Teaching Scheme:                            Examination Scheme:
Lect- 03hr                                   Theory Paper - 100 marks
Tutorial- 01hr                                TW - 25 marks

1  **8Bit Microcontroller**: Overview of 8051 microcontroller, architecture, instruction set, interfacing concept. 6

2  **16Bit Microcontrollers**: Introduction to MCS96 family, 8X196 - Architecture: CPU Block diagram, Memory, Special function Registers. 8

3  **Peripherals**: High speed input, High speed output, Interrupts, ADC, PWM, Timers, Serial port, I/O Port. Programming, Addressing Modes, Instruction Set, Programming, Comparison of various families of 16bit Microcontrollers. 10

4  **Microcontroller based System Design**: Case study with reference to 80196 Microcontroller. A typical application design from requirement analysis through concept design, detailed hardware and software design using 80196 Microcontrollers. Timing Analysis. e.g. Digital camera 8

5  **Design, Development and Debugging Tools for Microcontroller based Systems**: Software tools like Cross assembler, compiler, debuggers, simulators and hardware tools like In Circuit Emulators (ICE), Logic Analyzers etc. 4

Reference Books:
1  Intel Data Sheet 8X196
MS02: ADVANCED DIGITAL SYSTEM DESIGN

Teaching Scheme: 
Lect- 03hr 
Tutorial- 01hr  
Examination Scheme:  
Theory Paper - 100 marks  
TW - 25 marks  

1. **Review of logic design fundamentals:** Combinational logic, logic simplification, Quine McClusky minimization, Hazards in combinational networks.  
2. **Sequential machines:** Concept of memory, design of clocked flip flops, practical clocking aspects concerning flip flops, clock skew, traditional approaches in sequential machine analysis and design, Reduction of state tables and state assignments.  
3. **Asynchronous FSM:** Designing, cycles and races, hazards-static, dynamic and essential Hazards.  
4. **Computer Arithmetic:** Design of fixed point, floating point arithmetic units, MAC and SOP, CORDIC architectures.  
5. **Design using VHDL:** Entities and architectures, Data objects, types, design description, libraries, synthesis basics, mapping statements to Gates, model optimization, verification, test benches, Architectural synthesis, optimization, data path synthesis, logic level synthesis and optimization Cell library binding  
6. **Hardware testing and design for testability (DFT), FPGA:** Fundamental concepts, technologies, origin, alternative FPGA architectures, Configuration, Comparison with ASICs, Reconfigurable computing, Field Programmable node arrays, signal integrity and deep sub micron delay effects.  

REFERENCES:  
1. William I Fleatcher, An Engineering approach to digital design, PHI  
2. Giovanni De Micheli, Synthesis amd optimization of digital circuit (McGraw Hill)  
3. Charles H Roth, Jr., Fundamentals of Logic Design, Jaico Book  
5. Kevin Skahill, VHDL for programmable Logic, Addison Wesley  
# MS03: DIGITAL SIGNAL PROCESSORS & APPLICATIONS

**Teaching Scheme:**

<table>
<thead>
<tr>
<th>Lecture</th>
<th>Hours</th>
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<tbody>
<tr>
<td>1</td>
<td>03</td>
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<tr>
<td>2</td>
<td>01</td>
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**Examination Scheme:**

<table>
<thead>
<tr>
<th>Paper</th>
<th>Marks</th>
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<tbody>
<tr>
<td>Theory Paper</td>
<td>100</td>
</tr>
<tr>
<td>TW</td>
<td>25</td>
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1. **Architectures of Programmable DSP:** Basic Architecture, Computational building blocks, Bus Architecture, Addressing modes, Instruction set, Programming and Memory Interfacing.

2. **Commercial DSP TMS32054XX and TMS32067XX processors:** Architecture Programming and Interfacing.

3. **Filter design techniques:** Preliminary Considerations, Design of IIR filters, Impulse invariance, bilinear transformation, Design of FIR filters by windowing and frequency sampling.


5. **Multirate Digital Signal Processing Fundamentals:** The Basic Sample Rate Alteration Devices, Multirate Structures for Sampling rate conversion, Multirate design of Decimator and Interpolator, The poly phase decomposition, Arbitrary-rate sampling rate converter, Nyquist filter.

6. **Study of CCS:** Implementation of FIR and IIR filters, CODEC implementation, Speech processing applications, FFT algorithms on these processors.

**Reference Books:**

2. Digital Signal Processing- Jonathan Stein
3. Texas Instruments--TMS320C62x Image/Video Processing Library, Programmer’s Reference
Review of MOS Transistor Theory: nMOS and pMOS Enhancement transistor, Threshold voltage equations, Body effects, MOS device Design equations, Basic DC equations, Latch-up in CMOS circuits and other second order effects, MOS Models, depletion MOS.

Introduction to CMOS circuits: CMOS Logic- Complementary CMOS inverter- DC Characteristics, Noise margin, Static load MOS Inverters, Differential Inverter, the transmission gate, Tristate Inverter, Bi-CMOS Inverters, SPICE Model; Combination logic- static and dynamic design strategies, The NAND and NOR Gates, Compound gates, Multiplexers.

Designing Sequential logic circuits: Static latches and registers, Dynamic latches and registers, non bistable sequential circuits.

CMOS subsystem design: Adder, Multiplier, Shifter, other arithmetic operators; power and speed tradeoffs; Memory cells and Arrays, ROM, RAM- SRAM, DRAM, clocking disciplines; Design, power optimization, case studies in memory design.

CMOS Processing Technology: Basic CMOS technology, n and p well processes, CMOS Process Enhancements, Layout design rules, layouts of various gates, Technology related CAD issues.

Circuit Performance Parameters: Resistance and capacitance estimation, Inductance; Switching characteristics- analytical, empirical delay models, gate delays, CMOS Gate transistor sizing, Zpu/Zpd, Power dissipation, Sizing routing conductors, Charge sharing, Yield, reliability, Scaling of MOS Transistor dimensions.

REFERENCES:
5. Ivan Sutherland, Morgan Kaufeman, ‘Logical effort’, CA.
Introduction: Digital image representation, fundamental steps in image processing, elements of digital image processing systems, hardware for image processing system, Frame Grabber, Characteristics of image digitizer, Types of digitizer, Image digitizing components, Electronic image tube cameras, solid state cameras, scanners, Elements of visual perception, a simple image model sampling and quantization some basic relationship between pixels, image geometry, Basic transformations, perspective transformation, camera model and calibration, stereo imaging.

Image transforms: 2-D Fourier transform, Fast Fourier transform, Other separable transforms: Walsh Transform, Hadamard Transform, Discrete Cosine Transform, wavelet Transform, Haar function, Gabor Transform, Hotelling transforms.

Image enhancement: Enhancement by point processing, spatial filtering, enhancement in the frequency domain, Color image processing.

Image compression: Redundancies, image compression models, elements of information theory, error-free compression variable length coding, bit plane coding, lossless predictive coding, lossy compression, predictive coding, transform coding, video compression, image compression standards- JPEG, MPEG.

Image Analysis: Segmentation, detection of discontinuities, edge linking and boundary detection, thresholding, region -oriented segmentation,


2-D Motion Estimation: Optical flow, General Methodologies, Pixel Based based motion estimation, block-matching Algorithm, Mesh based motion Estimation, Global Estimation, Region based Motion estimation, Application of motion Estimation in video coding, Video standards H.263/264, MPEG-2 etc

REFERENCES:
5. Yao Wang, Joern Ostermann, Ya-Qin Zhang, Video Processing in Communication.
MS05(b): RF AND MIXED-SIGNAL INTEGRATED CIRCUITS

Teaching Scheme:
Lect- 03hr Theory Paper - 100 marks
Tutorial- 01hr TW - 25 marks


2. **Voltage Reference:** Review of diode behavior, Diodes and Bipolar Transistors in CMOS technology, Supply-independent bias circuits, Band gap voltage reference, Constant-gm bias.


3. **Mixers:** Mixer fundamentals, Non-linear systems as linear mixers, Multiplier-based mixers, Sub-sampling mixers, Diode-ring mixers. RF Power Amplifiers: Classes of power amplifiers, RF power amplifier design example, Power amplifier characteristics and Design consideration. Phase-Locked Loops (PLL): Introduction to PLL, Linearized PLL models, Some noise properties of PLLs, Phase detectors, Sequential phase detectors, Loop filters and charge pumps, PLL design examples. Oscillators and Synthesizers: Problems with purely linear oscillators, Describing functions, Resonators, Tuned oscillators, Negative resistance oscillators, Frequency synthesis.

REFERENCES:
MS05(c): STATISTICAL SIGNAL PROCESSING

Teaching Scheme: Examination Scheme:
Lect- 03hr Theory Paper - 100 marks
 Tutorial- 01hr TW - 25 marks


REFERENCES:
1  Monson H. Hayes, Statistical Digital Signal Processing & Modeling, John Wiley & Sons
MS06: SYSTEM LAB-I

Teaching Scheme:
Practical - 04hr/week

Examination Scheme:
Pract - 25 marks

Individual candidate or group of two (max) candidates will perform the work as per following and submit the report based on result obtained and/or study performed under the guidance of respective guide (minimum 25 pages).

The work will be assessed by an oral / practical examination of two hours duration by two examiners, out of which one will be respective guide or the teacher nominated by head of the department in the absence of respective guide on schedule. Second examiner will be eminent teacher or professional/expert from industry.

Work to be carried out by the student:

1. Candidate will perform experimentation in any subject laboratory of the department/Institute as assigned by the respective guide, leading towards concept understanding, development of laboratory set up and/or learning resources.

   OR

2. Candidate will perform literature survey about the topic and/or concerned subject laboratory assigned by respective guide, leading towards the detailed report for modernization, research and development or thrust area subject laboratory. (Thrust area should be as per Govt. of Maharashtra/ Govt of India Policies and AICTE/UGC/DST/DRDO/ISRO etc. guide lines).

   OR

3. Candidate will develop, specific software using c/c++/VB/VC/Java etc. which will improve functioning of the system. (subject laboratory/Library/Student section/office/Exam System etc.)

   OR

4. Candidate will perform detailed hardware and software designing of product/system/concerned to the subject laboratory leading towards post graduate dissertation.
MS07: EMBEDDED SYSTEM DESIGN

Teaching Scheme:  
Lect- 03hr  
Tutorial- 01hr

Examination Scheme:  
Theory Paper - 100 marks  
TW - 25 marks

1. **Introduction:** Embedded systems overview, Design Challenges, Processor Technology, IC Technology, Design Technology, Trade-offs, Custom Single purpose processors, RT level Custom Single purpose processor design, Optimization, General Purpose processors: pipelining, superscalar and VLIW architectures, Programmers view: Instruction set, program and data memory space, I/O, interrupts, operating system, Development environment: design flow and tools, testing and debugging, Application specific instruction set processors (ASIPs), microcontrollers, digital signal processors, less-general AIP environments, selecting microprocessors, general purpose processor design


3. **Peripherals:** Introduction, timers, counters and watchdog timers, UART, Pulse width modulators, controlling a DC motor using PWM, LCD controllers, Keypad controllers, stepper motor controllers, ADCs, Real time clocks

4. **Memory:** memory write ability and storage permanence, common memory types, composing memory, memory hierarchy and cache, advanced RAM.

5. **Interfacing:** introduction, Communication basics, Basic protocol concepts, ISA bus protocol: memory access, Arbitration, Priority arbiter, Daisy chain Arbitration, wireless communication, Layering, error detection and correction, wireless protocols: IrDA, Bluetooth, IEEE802.11

6. **RTOS:** Introduction Real Time operating systems: CSP Model, Process, Threads, process scheduling, examples of RTOS.

REFERENCES:

2. Dr.K.V.K.K.Prasad ‘Embedded Real Time Systems’ Dreamtech
3. Andrew Sloss Embedded System Developers’
4. Frank Vahid and Tony Givargis, Embedded system design: A unified hardware/software introduction, John Wiley and Sons, 2002
MS08: ADVANCED COMPUTER ARCHITECTURE

Teaching Scheme:          Examination Scheme:
Lect- 03hr                Theory Paper - 100 marks
Tutorial- 01hr            TW - 25 marks

1 Fundamentals of Computer Design: Introduction to computer design, Changing face of computing and task of computer designer, Technology trends, Cost, price and their trends, Measuring and reporting performance, Quantitative principles of computer design, RISC versus CISC, Major organizational issues of processor design: data path and control design.

2 Instruction set principles: Introduction, Classifying instruction set architectures,

3 Memory addressing, Addressing modes for signal processing, Type and size of operands and operations, type of operands and operations for media and signal processing, Instructions for control flow, encoding of an instruction set, Role of compilers, MIPS architecture, fallacies and pitfalls.

4 Instruction level parallelism and it’s dynamic exploitation: Instruction level Parallelism: concepts and challenges, overcoming data hazards with dynamic scheduling, Basic and intermediate concepts of pipelining: Introduction, the major hurdle of pipelining, RISC pipelined data path.

5 Memory Hierarchy Design: Introduction, Review of ABCs of caches, cache performance, reducing cache miss penalty, reducing cache miss rate, reducing cache hit time, virtual memory: protection and examples of virtual memory.

6 Parallel processing: Trends towards parallel processing, parallelism in uniprocessor systems, classification of parallel computers and their structures, applications of parallel processing.

REFERENCES:
1 John L. Hennessy and David A. Patterson, Computer Architecture, A Quantitative Approach (2nd Ed.), Morgan Kaufmann
2 P. Chaudhuri, Computer Organization and Design (2nd Ed.), PHI
4 Kai Hwang and Fay’e A. Briggs, Computer Architecture and Parallel Processing, Mc Graw Hill.
MS09: VLSI DIGITAL SIGNAL PROCESSING SYSTEMS

Teaching Scheme:  
Lect- 03hr  
Tutorial- 01hr  

Examination Scheme:  
Theory Paper - 100 marks  
TW - 25 marks

1 Introduction to DSP System: Typical DSP algorithms, DSP application demands and scaled CMOS technology, Representation of DSP algorithms.

   Iteration Bound: Data-flow graph representations, Loop bound and iteration bound, Algorithms for computing iteration bound, Iteration bound of multirate data-flow graphs.

   Pipelining and Parallel Processing: Pipelining of FIR digital filters, Parallel processing, Pipelining and parallel processing for low power.

   Retiming: Definitions and properties, Solving systems of inequalities, Retiming techniques.

2 Unfolding: An algorithm for unfolding, Properties of unfolding, Critical path, unfolding and retiming, Applications of unfolding.

   Folding: Folding transformation, Register minimization techniques, Register minimization in folding architectures, Folding of multirate systems.

   Systolic Architecture Design: Systolic array design methodology, FIR systolic arrays, Selection of scheduling vector, Matrix-matrix multiplication and 2D systolic array design, Systolic design for space representations containing delays.

3 Bit-Level Arithmetic Architecture: Parallel multipliers, Interleaved floor-plan and bit-plane-based digital filters, Bit-serial multipliers, Bit-serial filter design and implementation, Canonic signed digit arithmetic, Distributed arithmetic.


Reference Books:


MS10: REAL TIME EMBEDDED OPERATING SYSTEM

Teaching Scheme:
Lect- 03hr
Tutorial- 01hr

Examination Scheme:
Theory Paper - 100 marks
TW - 25 marks

1. **Real-Time Systems Concepts**: real-time systems concepts such as foreground/background systems, critical sections, resources, multitasking, context switching, scheduling, reentrancy, task priorities, mutual exclusion, semaphores, intertask communications, interrupts and more.

2. **Kernel Structure**: Introduction to μC/OS-II and its internal structure. tasks, task states, task control blocks, how μC/OS-II implements a ready list, task scheduling, the idle task, Determination of CPU usage, μC/OS-II handles interrupts, Initialization and start μC/OS-II and more.

3. **Task Management**: μC/OS-II’s services to create a task, delete a task, check the size of a task’s stack, change a task’s priority, suspend and resume a task, and get information about a task.

4. **Time Management**: μC/OS-II Time Management Services

5. **Intertask Communication and Synchronization**: μC/OS-II’s services to have tasks and ISRs (Interrupt Service Routines) communicate with one another and share resources. semaphores, message mailboxes and message queues Implementation

6. **Memory Management**: μC/OS-II’s dynamic memory allocation feature using fixed-sized memory blocks.

7. **Porting μC/OS-II**: Porting of μC/OS-II to ARM_7TDMI processor architectures

8. **Application development using μC/OS-II and ARM Processor**

References:
2. Jean Lambrosse, Embedded System Building Blocks, R&D Books, Lawrence
4. Phillips, LPC-ARM Processor Application Notes
MS11(a) : RECONFIGURABLE COMPUTING

Teaching Scheme:                                             Examination Scheme:
Lect- 03hr                                                  Theory Paper - 100 marks
Tutorial- 01hr                                               TW - 25 marks

1  **Reconfigurable Architectures**: Simple Programmable Logic Devices, CPLDs, FPGAs, Coarse-Grained Reconfigurable Devices.

2  **Implementation and High level Synthesis**: Design flow, Modelling, Temporal Partitioning

3  **On line Communication**: Direct Communication, Bus Based Communication, Circuit Switching and Network on chip.


5  **System on Programmable Chip**: Introduction to SoPC, Adaptive Multiprocessing on Chip.

6  **Application**: Pattern matching, Adaptive Controllers.

**Reference:**
1  Introduction to Reconfigurable Computing Architectures, Algorithms and Applications by Christophe Bobda, Springer
2  Reconfigurable Computing – Maya Gokhale, Paul S. Graham
MS11(b): ADAPTIVE SIGNAL PROCESSING

Teaching Scheme:
Lect- 03hr
Tutorial- 01hr

Examination Scheme:
Theory Paper - 100 marks
TW - 25 marks


**Linear Prediction**: Forward Linear Prediction, Backward Linear Prediction, Properties of Prediction Error Filters.

2  **Method of Steepest Descent**: Basic Idea of Steepest-Descent Algorithm, Steepest-Descent Algorithm Applied to Wiener Filter, Stability of Steepest-Descent Algorithm, Limitations of Steepest-Descent Algorithm.

**Least-Mean Square Adaptive Filter**: Overview, LMS Adaptation Algorithm, Application, Comparison of LMS With Steepest-Descent Algorithm.

**Normalized Least-Mean Square Adaptive Filter**: Normalized LMS Filter as the Solution to Constrained Optimization Problem, Stability of the NLMS.

3  **Frequency-Domain and Subband Adaptive Filters**: Block Adaptive Filters.

**RLS Adaptive Filters**: Statement of Linear Least-Square Estimation Problem, Matrix Inversion Lemma, The Exponentially Weighted RLS Algorithm.

**Kalman Filter**: Recursive Minimum Mean-Square Estimation For Scalar Random Variable, Kalman Filtering Problem, Initial Conditions, Summary of Kalman Filter.

Reference Books:
1  Bernard Widrow and Samuel D. Stearns, Adaptive Signal Processing, Pearson Education

2  Simon Haykin, Adaptive Filter Theory (Fourth Edition), Pearson Education
MS11(c): ANALOG INTEGRATED CIRCUIT DESIGN

Teaching Scheme: Examination Scheme:
Lect- 03hr Theory Paper - 100 marks
Tutorial- 01hr TW - 25 marks

1 Introduction: The MOS Transistor, I-V Characteristics, Equivalent Circuits, Noise 13
Resistor, Capacitors and Switches: Integrated Resistors, Integrated Capacitors, Analog
Switches, Layout of Switches
Basic Building Blocks: Inverter with Active Load, Cascade, Cascade with Cascade Load, Source
Follower, Threshold Independent Level Shift, Improved Output Stages

2 Current and Voltage Sources: Current Mirrors, Current References, Voltage Biasing, Voltage 14
References
CMOS Operational Amplifiers: General Issues, Performance Characteristics, Basic
Architecture, Two Stage Amplifier, Frequency Response and Compensation, Slew Rate

3 Operational Amplifiers and OTAs: Design of Two Stage OTAs: Guidelines, Single Stage 13
Schemes, Class AB Amplifiers, Fully Differential Op-Amps, Micro-Power OTAs, Noise Analysis,
Layout
CMOS Comparators: Performance Characteristics, General Design Issues, Offset
Compensation, Latches

Reference Books:
   238032-2.
4. Phillip E. Allen and Douglas R. Holberg, CMOS Analog Circuit Design, Oxford University Press,
Individual candidate or group of two (max) candidates will perform the work as per following and submit the report based on result obtained and/or study performed under the guidance of respective guide (minimum 25 pages).

The work will be assessed by a oral/practical examination of two hours duration by two examiners, out of which one will be respective guide or the teacher nominated by head of the department in the absence of respective guide on schedule. Second examiner will be eminent teacher or professional/expert from industry.

Work to be carried out by the student:

1. Candidate will perform experimentation in any subject laboratory of the department/institute as assigned by the respective guide, leading towards concept understanding, development of laboratory set up and/or learning resources.

OR

2. Candidate will perform literature survey about the topic and/or concerned subject laboratory assigned by respective guide, leading towards the detailed report for modernization, research and development or thrust area subject laboratory. (Thrust area should be as per Govt. of Maharashtra/Govt of India Policies and AICTE/UGC/DST/DRDO/ISRO etc. guide lines).

OR

3. Candidate will develop, specific software using c/c++/VB/VC/Java etc. which will improve functioning of the system(subject laboratory/Library/Student section/office/Exam System etc.)

OR

4. Candidate will perform detailed hardware and software designing of product/system/concerned to the subject laboratory leading towards post graduate dissertation.
SEMESTER-III
MS13: DISSERTATION SEMINAR

Teaching Scheme: Practical - 24hr
Examination Scheme: TW - 100 marks

The dissertation-Seminar will consist of type written report covering the topic selected for Dissertation project. The candidate shall deliver the seminar on the topic which will be judged by two examiners.

SEMESTER-IV
MS14: DISSERTATION

Teaching Scheme: Practical - 24hr
Examination Scheme: TW - 200 marks

Practical Examination
The practical examination will consist of a presentation alongwith the demonstration of the project. The said examination will be conducted by a panel of two examiner(one internal guide and one external examiner)